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SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE
SENSOR (AS AMENDED)

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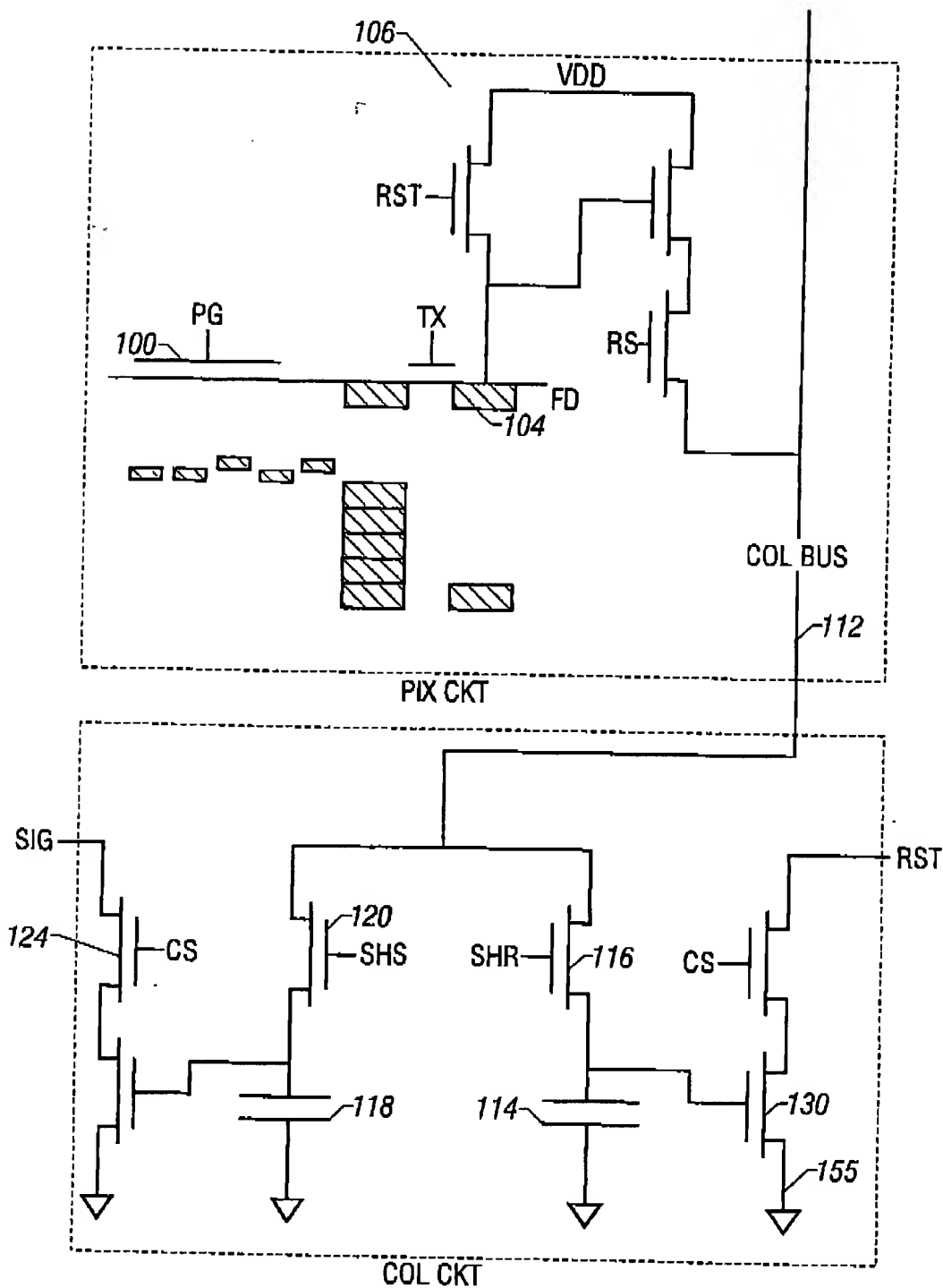


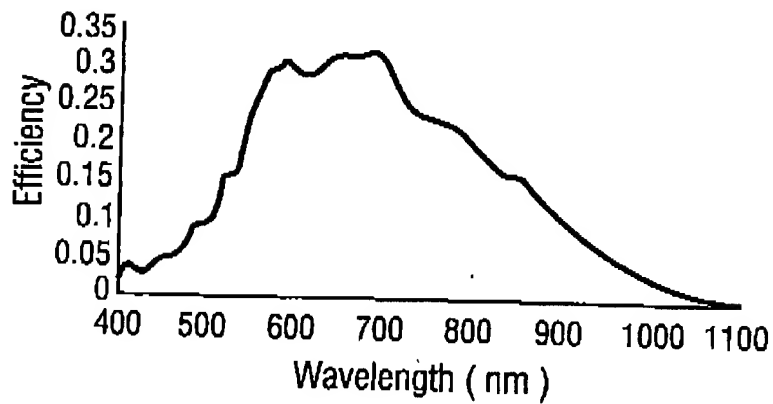
FIG. 1

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SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE
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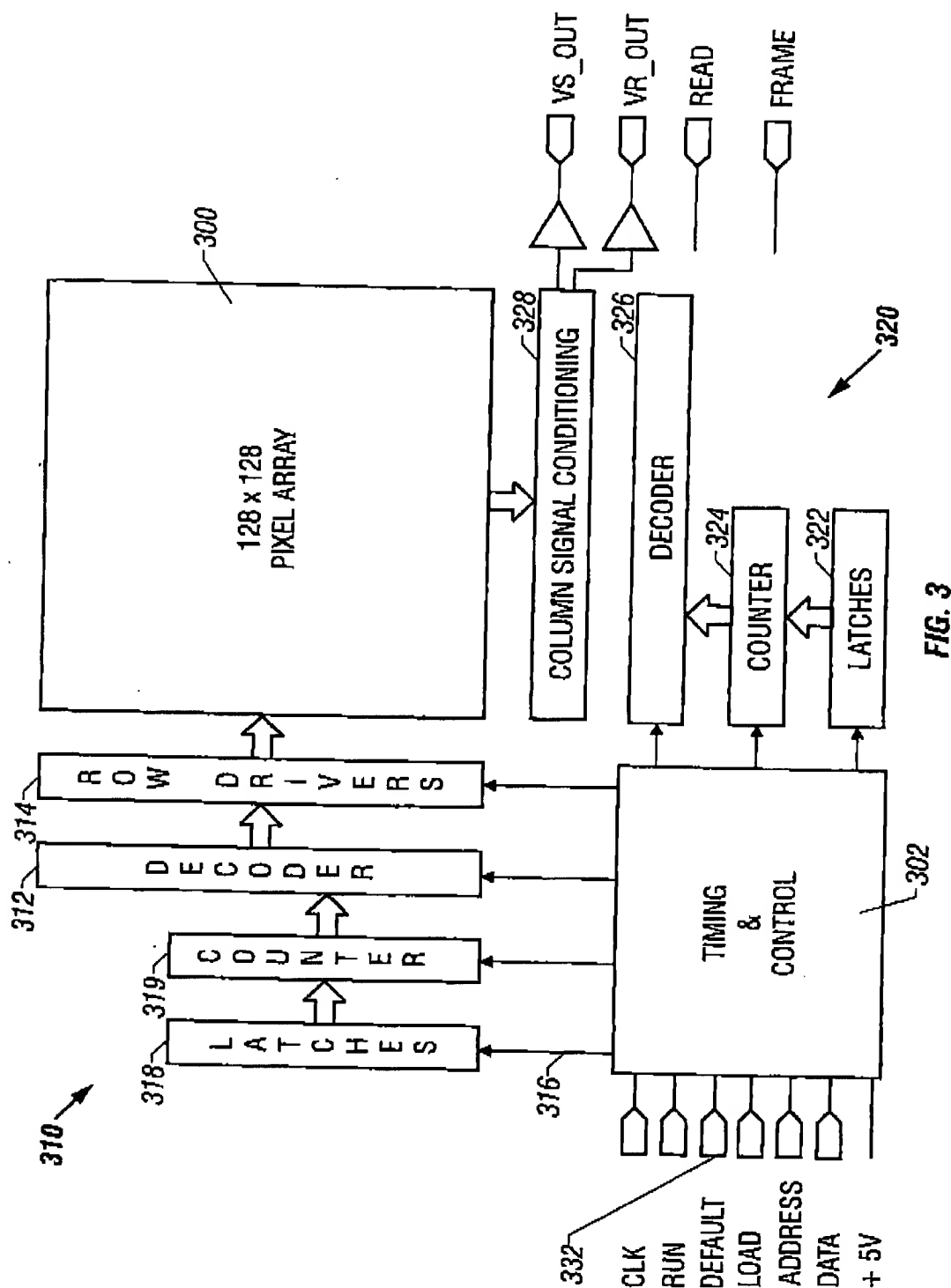
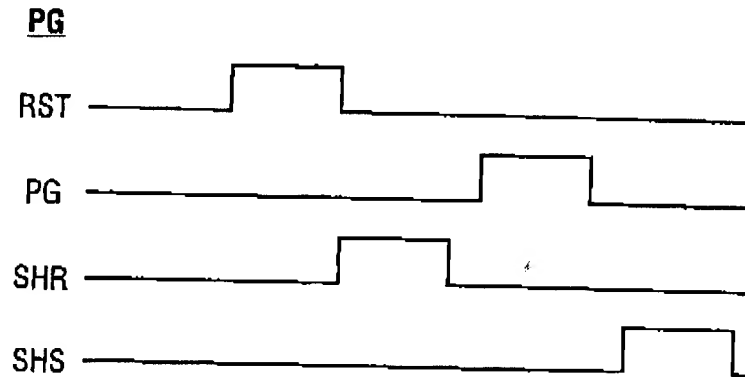
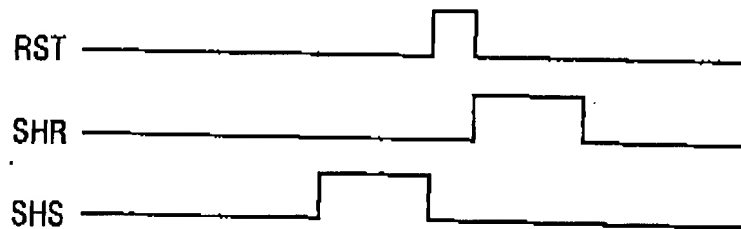


FIG. 3

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4/10**FIG. 4A****FIG. 4B**

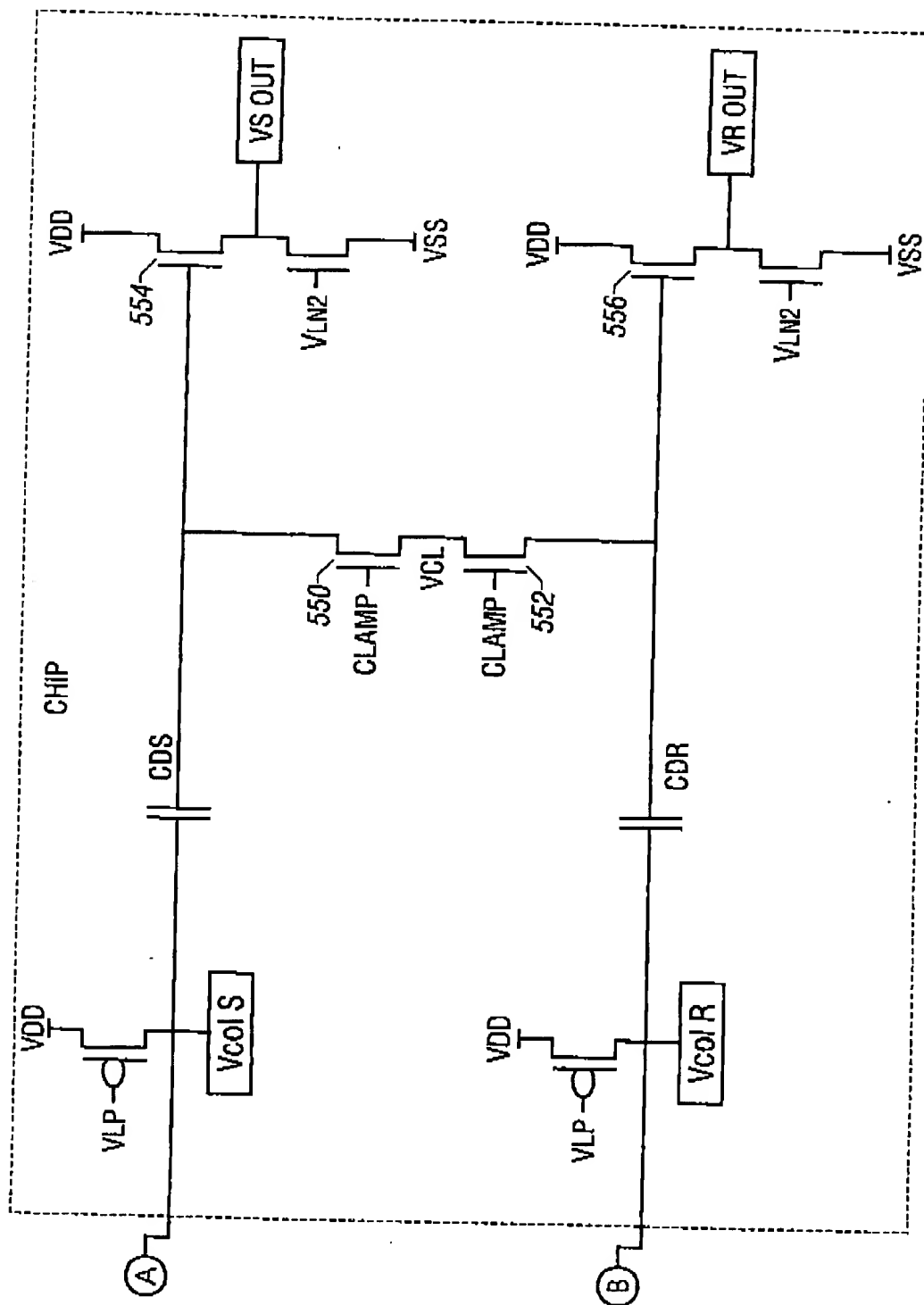
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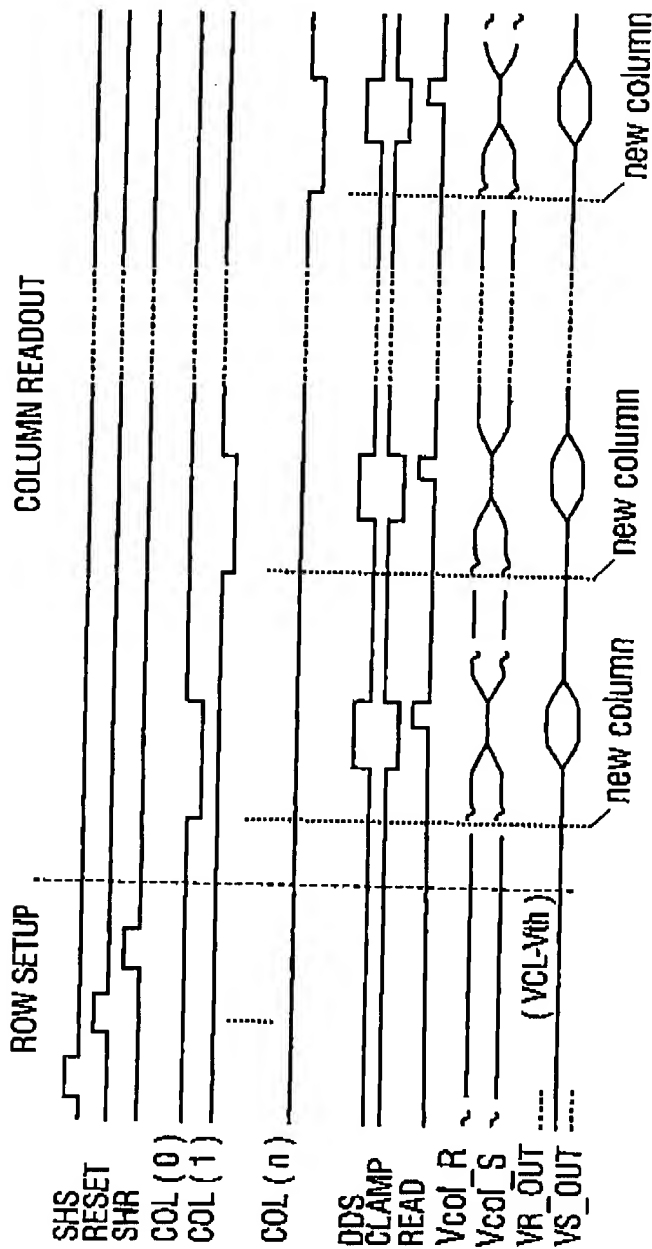
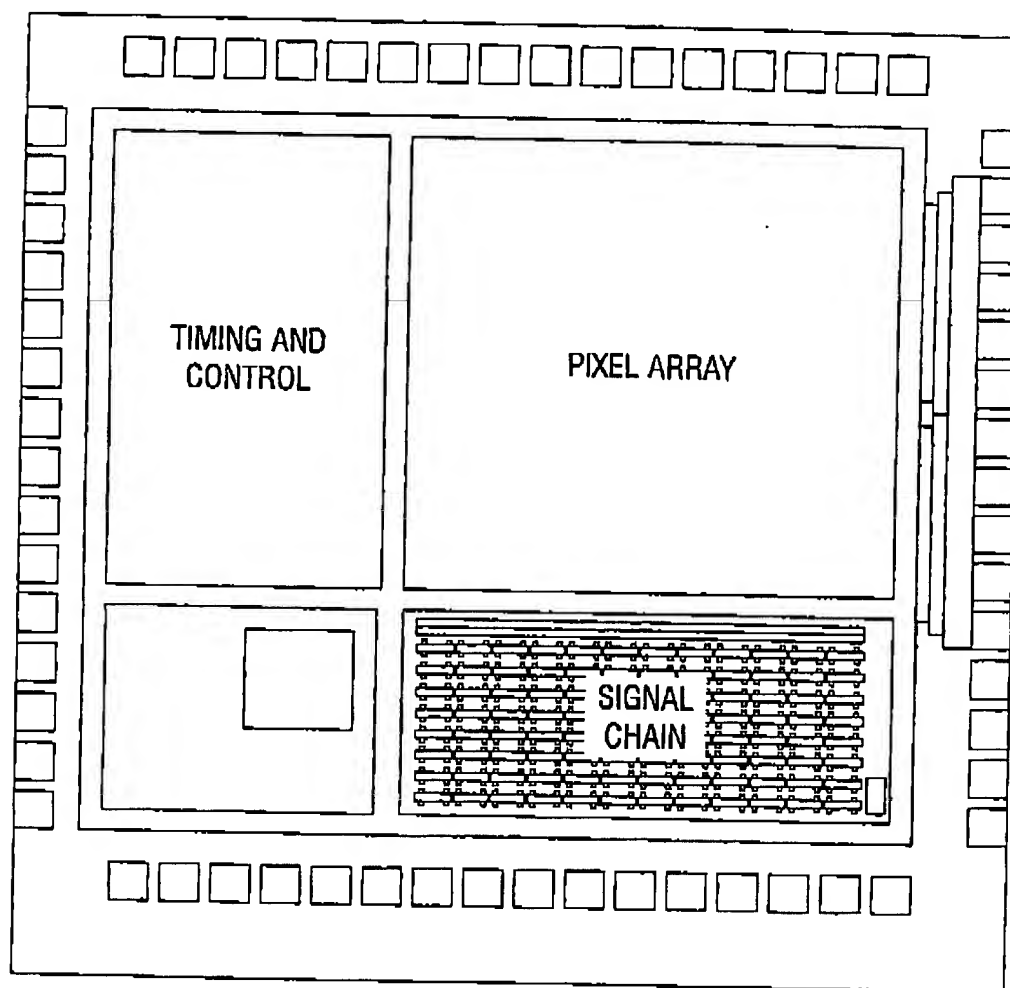


FIG. 6

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SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE
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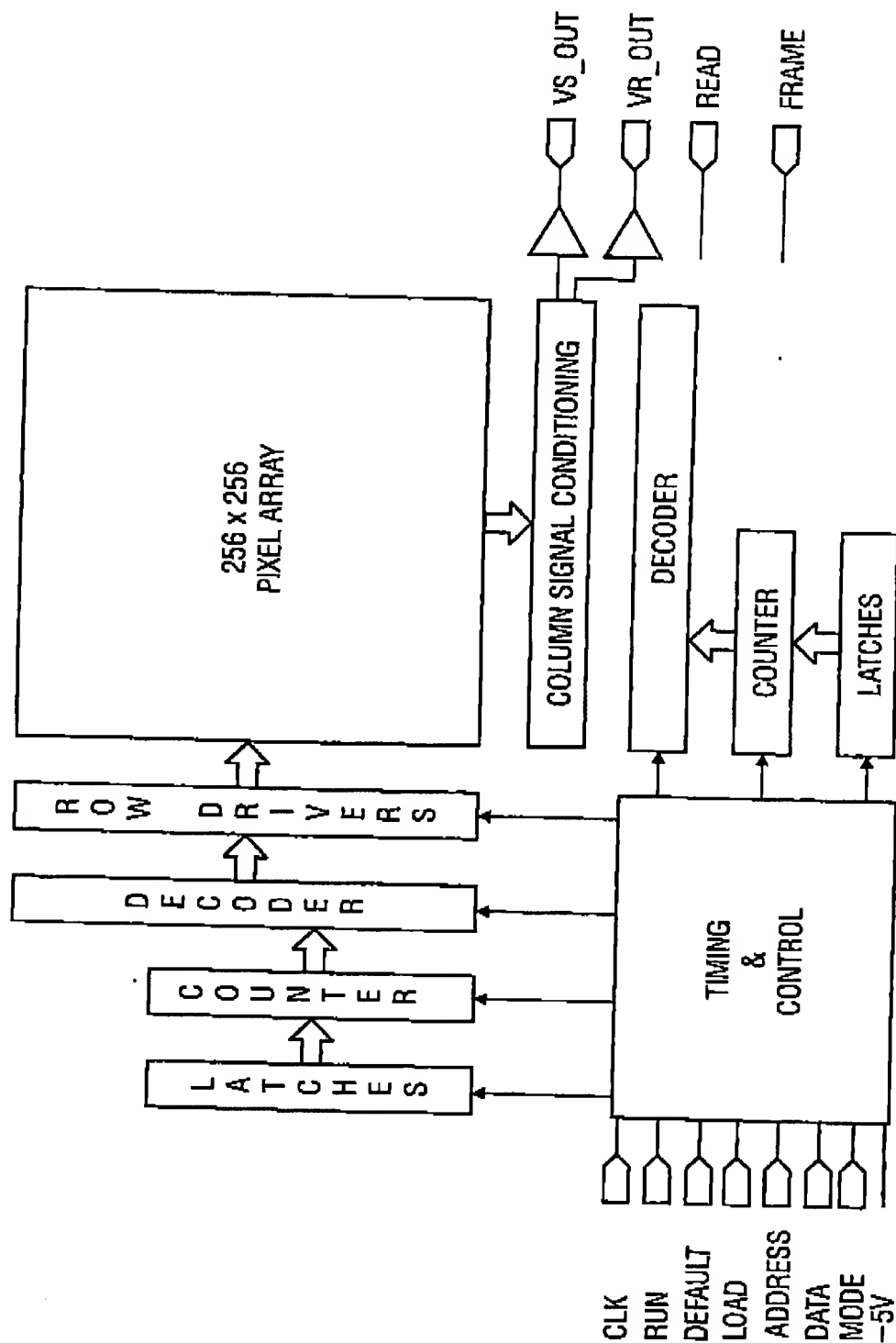
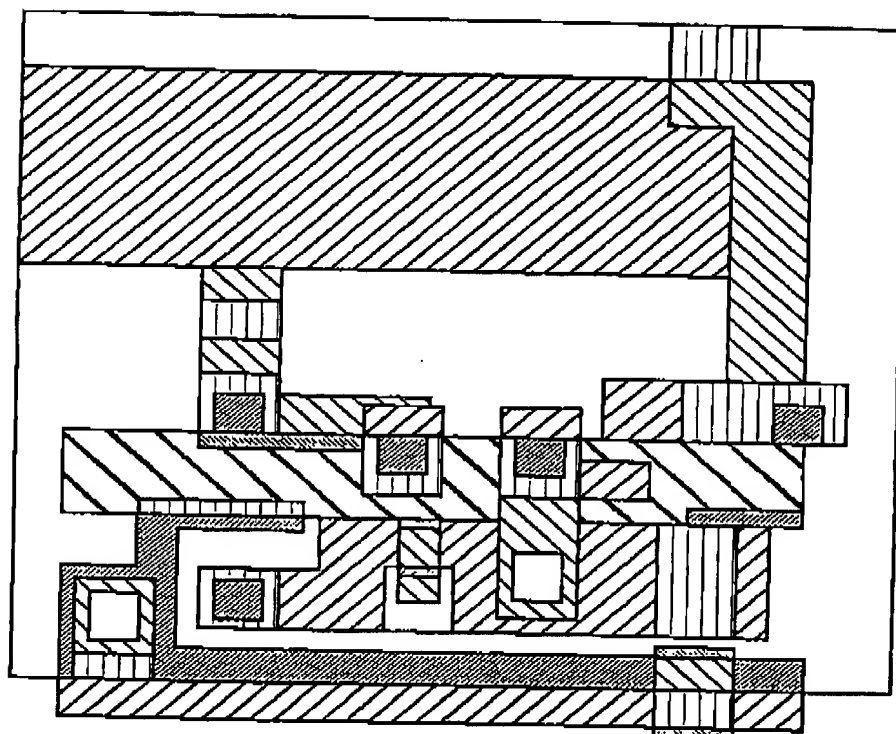


FIG. 8

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Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10 ⁹ clock periods or 1600 secs at 10 MHz

FIG. 8